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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/511,931	02/24/2000	Takayuki Sugawara	9281-3561	5649

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EXAMINER

BAKER, STEPHEN M

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/511,931	Applicant(s) SUGAWARA ET AL.	
	Examiner Stephen M. Baker	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 July 2005.
- 2a) ☒ This action is **FINAL**.      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-10 is/are rejected.
- 7) ☒ Claim(s) 2 and 3 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

*AT*

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. Claims 1 and 4-10 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,737,344 to Belser *et al* (hereafter Belser '344).

Belser '344 discloses error correction for a data read from a disk drive of a computer system by using parity sectors whenever a sector-level ECC process is unsuccessful (col. 6, lines 61-67, etc). Belser '344's disk drive (200), in the conventional manner, includes a head (218) for reading data written to the disk (220), and a processing circuit (202) for processing the read data. Belser '344's computer system includes a "host computer" (212) that is "connected to said disk drive through an interface" (210). A first level of Belser '344's error correction processing (col. 3, lines 53-58) is performed by an ECC unit (214), within the disk drive unit, over individual data blocks, wherein each data block is a sector (col. 4, lines 27-30). Accordingly, Belser '344's ECC unit (214) is a "low-level error-correction unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk". The second level of Belser '344's error correction processing can be performed (col. 5, lines 63-66) by the host computer (212) to correct data of multiple (two) sector-level-ECC-uncorrectable sectors, by using more than a single parity sector coding (col. 7, lines 1-16) to provide a second-level ECC process more robust than is possible with a

single parity sector. Accordingly, Belser '344's host computer (212) "includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk".

Regarding claims 5-7, each of Belser '344's sectors corresponds to a "physical address".

Regarding claim 8, both levels of Belser '344's error correction share "common" sectors.

### ***Claim Rejections - 35 USC § 103***

3. Claims 1 and 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,021,463 (hereafter "Belser '463") in view of Belser '344.

Belser '463 discloses error correction for a data read from a disk drive of a computer system by using parity sectors whenever a sector-level ECC process is unsuccessful. Belser '463's disk drive, in the conventional manner, includes a head for reading data written to the disk, and a processing circuit for processing the read data. Belser '463's computer system includes a "host computer" (1) that is "connected to said disk drive through an interface" (23, etc). A first level of Belser '463's error correction processing is performed by an ECC unit (27), within the disk drive unit, over individual data blocks, wherein each data block is a sector (col. 3, lines 5-30). Accordingly, Belser '463's ECC unit (27) is a "low-level error-correction unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk". A second level of Belser '463's error correction processing is performed by a disk drive

processor (9) to correct data of multiple sector-level-ECC-uncorrectable sectors, by using more than a single parity sector (col. 6, lines 48-59) to provide a second-level ECC process more robust than is possible with a single parity sector. Accordingly, Belser '463's disk drive processor (9) "includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk", rather than the host computer (1).

Belser '344 teaches that a second level of ECC processing may be provided in the host computer instead of in the disk drive processor (col. 5, lines 63-66). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the ECC system disclosed by Belser '463 by placing the second-level ECC processing in the host computer (1) instead of the disk drive processor (9). Such a modification would have been obvious because Belser '344 teaches that a second level of ECC processing may be provided in the host computer instead of in the disk drive processor.

Regarding claims 5-7, each of Belser '463's sectors corresponds to a "physical address".

Regarding claim 8, both levels of Belser '463's error correction share "common" sectors.

***Allowable Subject Matter***

4. Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

5. Applicant's arguments filed 11 July 2005 have been fully considered but they are not persuasive.

Applicant suggests that Belser '344 fails to teach whether the ECC process is performed at the disk drive (hardware) level and whether the parity sector correction is performed at the host computer (software) level. Regarding applicant's suggestion that Belser '344's host (212) software does not perform error correction using the parity sector, Belser '344 makes it clear that the host (212) may perform the encoding algorithm for generating the parity sector data ("tasks 600 may be performed by ... a host computer" – Belser '344, col. 5, lines 64-65) and furthermore Belser '344 indicates that the corresponding decoding algorithm for using the parity sector data to correct errors found uncorrectable at the sector level may be performed by the same means used to perform the parity sector encoding algorithm ("tasks 700, *like the tasks 600*, may be performed ... as discussed above" – Belser '344, col. 6, lines 22-23). Regarding applicant's suggestion that Belser '344's disk drive hardware does not perform an ECC decoding process, Belser '344 makes it clear that ECC is provided in each sector (col. 1, lines 61-62) and that a hardware unit (214) in the disk drive may perform the in-sector

ECC decoding (col. 3, lines 53-58) using Reed-Solomon code, which is of course the standard ECC coding for in-sector ECC. Belser '344 *in no way* suggests that the host computer should also perform the in-sector ECC, and so applicant cannot provide any citation from Belser '344 to show otherwise.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

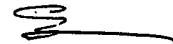
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Stephen M. Baker  
Primary Examiner  
Art Unit 2133

smb